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Substitute for form 1449/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	10/684,713		
		Filing Date	10/14/2003		
		First Named Inventor	Paul Arthur Layman		
		Art Unit	2811		
		Examiner Name	Unassigned		
Sheet	2	of	2	Attorney Docket Number	Chaudhry 25-18-8-12-5/075903-282

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
RP	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
RP	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	
RP	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
RP	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEDM 1988, pp. 222-225.	
RP	5	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.	
RP	6	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs", IEEE 2000.	
	7	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.	
RP	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	

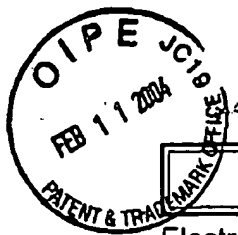
Examiner Signature	<i>for Pompey</i>	Date Considered	6-28-03
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor						
<div>Application Number: 10/684713</div> <div>Confirmation Number: 4836</div> <div>First Named Applicant: Paul Layman</div> <div>Attorney Docket Number: 075903-282</div> <div>Art Unit: 2811</div> <div>Search string: (4670768 or 5010386 or 5140388 or 5502009 or 5861347 or 6300199 or 6309930 or 6387758 or 4366495 or 4455565 or 4587713 or 4683643 or 4786953 or 4837606 or 5342797 or 6027975 or 6072216 or 6133099 or 6197641 or 6133164 or 5414289 or 5576238 or 5668391 or 5744846 or 6297531 or 4951102 or 5208172 or 5545586 or 5554870 or 5864158 or 6268621).pn.</div> <div></div>							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
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	2	5010386	1991-04-23	Groover, III			
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	15	5342797	1994-08-30	Sapp, et al
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	18	6133099	2000-10-17	Sawada
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	28	5545586	1996-08-13	Koh
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	30	5864158	1999-01-26	Liu, et al
RP	31	6268621	2001-07-31	Emmi, et al

Signature

Examiner Name	Date
Rm Pompey	6-28-05